

DATA PROCESSING APPARATUS

ABSTRACT OF THE DISCLOSURE

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A data processing apparatus which downloads a corrective program into its RAM during initial program loading, performs by its CPU interrupt processing in response to an interrupt request signal output from a debugging circuit when a program address coincides with a predetermined bug address, executes the debugged program, then reads program codes from the memory address next to the buggy part of a program to continue the processing after the interrupt processing. By executing the debugged program stored in the RAM as an interrupt processing routine instead of executing the buggy part of the program stored in the ROM, the buggy program is replaced by the bug-free corrected program and therefore the bug can be avoided.

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